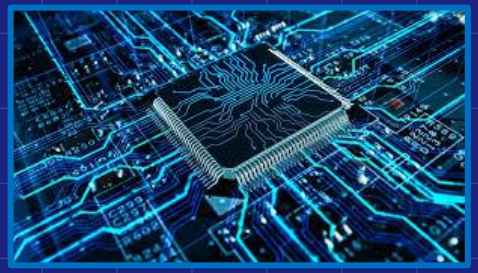
UNIVERSITAT POLITÈCNICA DE VALÈNCIA

DISCA
DEPARTAMENTO DE INFORMÁTICA DE SISTEMAS Y COMPUTADORES

Las Charlas del Máster

Máster en Ingeniería de Computadores y Redes



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José Duato Marín
OpenChip

[12/02/2026]
12.30 a 14.00
Aula Máster DISCA

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Conferencia Magistral 01

Advanced interconnect solutions for high-performance AI accelerators

Resumen de la Charla

The massive deployment of increasingly larger LLM models has triggered the design of advanced accelerators to provide the required computational power. Those accelerators implement HBM memory to provide the required memory bandwidth, which drastically limits memory capacity per accelerator. As a consequence, LLM models have to be spread among multiple accelerators, leading to previously unexisting communication needs. This talk introduces the different kinds of interconnects that exist in state-of-the-art datacenters and their main features. It also addresses power consumption and the need for advanced solutions to make datacenters more sustainable.

Sobre el Ponente

José Duato has been a professor at the Polytechnic University of Valencia for 41 years, where he has developed solutions that have been patented and/or incorporated into multiple processors, supercomputers, and communications standards. He is currently Director of System Architecture at Openchip and a Full Member of the Royal Academy of Exact, Physical and Natural Sciences of Spain. He has been awarded the Rei Jaume I Prize for New Technologies, the Aritmel National Prize for Computer Science, and the Julio Rey Pastor National Prize for Research in Mathematics and Information and Communications Technologies. He is the author of more than 500 publications with over 18,900 citations and a dozen international patents. He coauthored the textbook "Interconnection Networks: An Engineering Approach" and the appendix on "Interconnection Networks" in the famous Hennessy & Patterson textbook.

Conferencia Magistral 02

La verificación en un entorno empresarial

Resumen de la Charla

In a company, during the different stages of a project for a hardware design product several engineer teams contribute to different aspects, like development, documentation, etc. In this session, Samuel will go through those different aspects and the details on how the team of verification engineers can contribute. One key takeaway from this talk is to show that verification effort is pervasive to all project phases

Sobre el Ponente

Samuel Rodrigo Mocholí obtuvo su título de Ingeniero en Informática en el 2005, y posteriormente su grado de Doctor en 2010. Ambos en la Universitat Politècnica de València (UPV), España. Durante su doctorado investigó principalmente en campos aplicados a Redes dentro del Chip. A través de su experiencia en el doctorado encontró la oportunidad de realizar una estancia postdoctoral en Simula Research Laboratory (Noruega), lo cual le permitió seguir la investigación en el mismo campo para el proyecto europeo NaNoC. Posteriormente se unió a Oracle, adquiriendo experiencia en verificación de hardware, principalmente en productos de red y aceleradores, pasando por otras empresas como Graphcore para el soporte de diseños de chips de inferencia. Actualmente es líder de equipo en Numascale, una empresa dedicada a la arquitectura, diseño y verificación de varios proyectos hardware que colabora con varias empresas internacionales dentro del campo de redes y computadores de altas prestaciones. Numascale ha abierto recientemente una oficina en Valencia, España.

Samuel Rodrigo Mocholí

[26/02/2026]
12.30 a 14.00
Aula Máster DISCA

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Carmen Garcia Almudever

[12/03/2026]
12.30 a 14.00
Aula Máster DISCA

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Conferencia Magistral 03

Una visión sistemática de la computación cuántica

Resumen de la Charla

The advances in quantum hardware with functional quantum processors integrating tens and even hundreds of noisy qubits, together with the availability of near-term quantum algorithms have allowed the development of the so-called full-stacks that bridge quantum applications with quantum devices. In this talk, after discussing the principles of quantum computing and the progress of this field, we will provide an overview of the different layers of the quantum computing full-stack, with emphasis on the software ones that include the compilation of quantum algorithms. We will then focus on key principles for architecting quantum computers such as codesign, optimization and benchmarking. Finally, we will talk about the scalability of quantum computers, which is one of the main challenges of current quantum computers.

Trayectoria

Carmen G. Almudever es profesora titular en el departamento de Informática de Sistemas y Computadores (DISCA) de la Universitat Politècnica de València (UPV), donde lidera el grupo de investigación en arquitecturas de computación cuántica. Con más de 10 años de experiencia en este campo, Carmen trabaja en el diseño y desarrollo de sistemas ‘full-stack’ de computación cuántica centrándose en diferentes áreas que incluyen: técnicas de compilación para la implementación eficiente de algoritmos cuánticos y aplicaciones de redes de comunicación cuántica, corrección de errores cuánticos y computación tolerante a fallos, quantum machine learning, arquitecturas modulares de gran escala y métodos de diseño y optimización.

Conferencia Magistral 04

Advanced Cloud-Native Architectures: from Service Mesh to Serverless

Resumen de la Charla

In this talk, we'll explore the core principles behind today's large-scale microservice deployments and the real-world challenges of running distributed, heterogeneous systems. We'll look at proven practices for designing, deploying, and maintaining resilient distributed architectures across a wide range of environments—from massive cloud platforms to IoT-driven infrastructures.
Building on these foundations, the talk highlights emerging cloud models and the tools reshaping how developers and operators manage complexity. We'll take a closer look at Service Mesh technologies and discuss how they streamline DevOps workflows in intricate microservice ecosystems. Finally, we'll examine the Serverless paradigm and its impact on modern development, showing how it frees teams to focus on business logic while benefiting from cloud-native scalability, efficiency, and operational simplicity infrastructure concerns, and leveraging cloud-native scalability and efficiency.

Sobre el Ponente

I'm Andrea Sabbioni (Graduate Student Member, IEEE, ACM), I received my M.Sc. degree (cum laude) in computer science engineering from the University of Bologna, Italy, where I pursued a Ph.D. degree in computer science and engineering. I'm currently holding a Junior Assistant Professor (fixed-term) position at the University of Bologna. My research interests include cloud, fog, and serverless computing, middleware, and architectural approaches for innovative tourism applications. My objective is to expand my current research on cloud computing and geo-distributed deployment scenarios to aid the reduction of the technological gap in the infrastructures supporting the growth of Smart Tourism offers.

Andrea Sabbioni

[16/04/2026]
12.30 a 14.00
Aula Máster DISCA

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