UNIVERSITAT POLITÈCNICA DE VALÈNCIA

SERVICIO INTEGRADO DE EMPLEO

SIEUPV

REF

E/49183/UPV

MaxLinear - ASIC Verification Engineer

EMPRESA

Servicios técnicos de ingeniería

FUNCIONES

MaxLinear is seeking an ASIC Verification Engineer to work from our Valencia, Spain Design Center. You will be responsible for the verification of communications / digital signal processing (DSP) SOCs. The subsystems include DSP functions, CPU subsystems, and peripheral interfaces. The ideal candidate will have an ASIC verification background with experience in SOC verification using leading edge verification tools and methods. Create verification specifications and plans Define block and top level test benches Execute to plans with simulation. Interesados incrpción en web: ASIC Verification Engineer - 1688-167

REQUISITOS

Required Skills Experience in verification strategy development and execution for large SoCs and signoff with coverage metrics Knowledge of UVM methodology and System Verilog. SystemC would be a plus Implementation of randomized and directed random testbenches for networking and multi-cpu environments Knowledge of verification IP and functional coverage techniques Experience with signoff of SoC designs with coverage metrics Able to ramp up with new technologies and products Experience with design would be a plus Strong logical and creative problem-solving skills with excellent analytical and debugging skills Flexible self-starter able to work effectively under pressure Good written and oral communication skills. Interesados incrpción en web: ASIC Verification Engineer - 1688-167

CONOCIMIENTOS/CURSOS SOLICITADOS

IDIOMAS SOLICITADOS

Inglés

CONDICIONES

Contrato indefinido, jornada completa. Salario según experiencia apartada. Fijo más varible. Interesados incrpción en web: ASIC Verification Engineer - 1688-167 <https://www.maxlinear.com/company/careers>

Zona de la oferta: Paterna

Fecha límite de la oferta: 08/08/2019

Interesados inscribirse en:
www.sie.upv.es/ofertas
96 387 78 88