# Efficient 0 1 0 ····· 0 1 0 1 ····· 1 0 0 1 ····· 0 : : : : : : : 0 1 0 ····· 1 Matrix Multiplications on RISC-V MCUs



Leverage Dot product vector instructions > New Multi-level **memory hierarchy** Approximate Computing > Modified BLIS (BLAS-like Library Instantiation Software)



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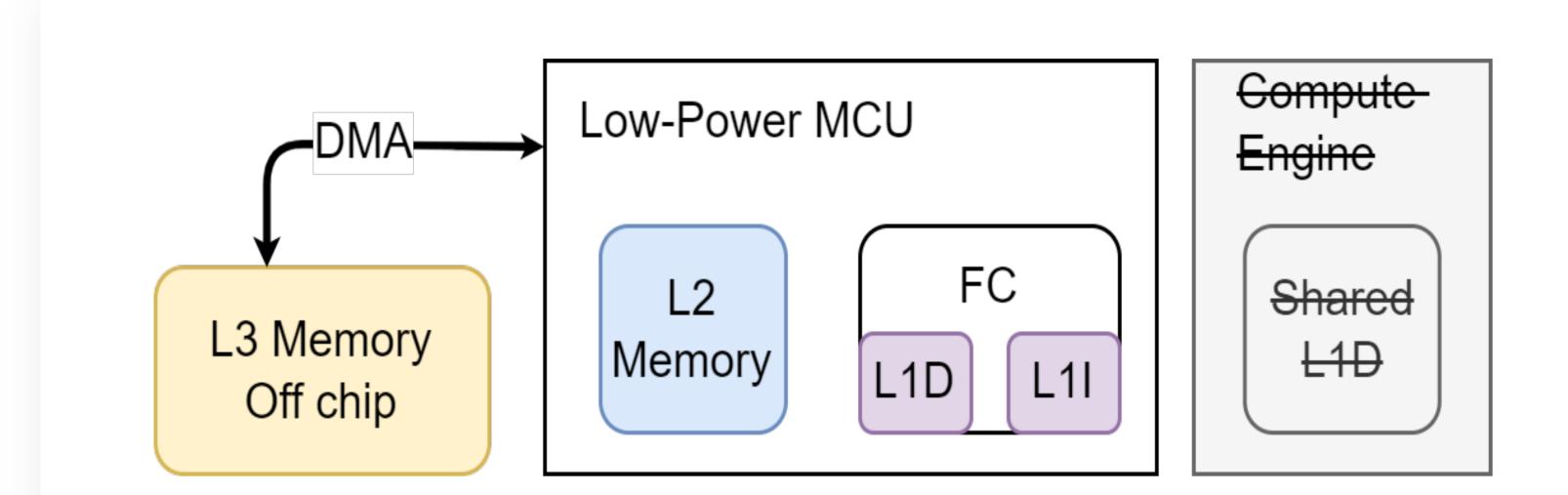




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Paper: Cristian Ramírez, Adrián Castellón, Enrique S. Quintana-Ortí. Poster: Cristian Ramírez, Jie Lei

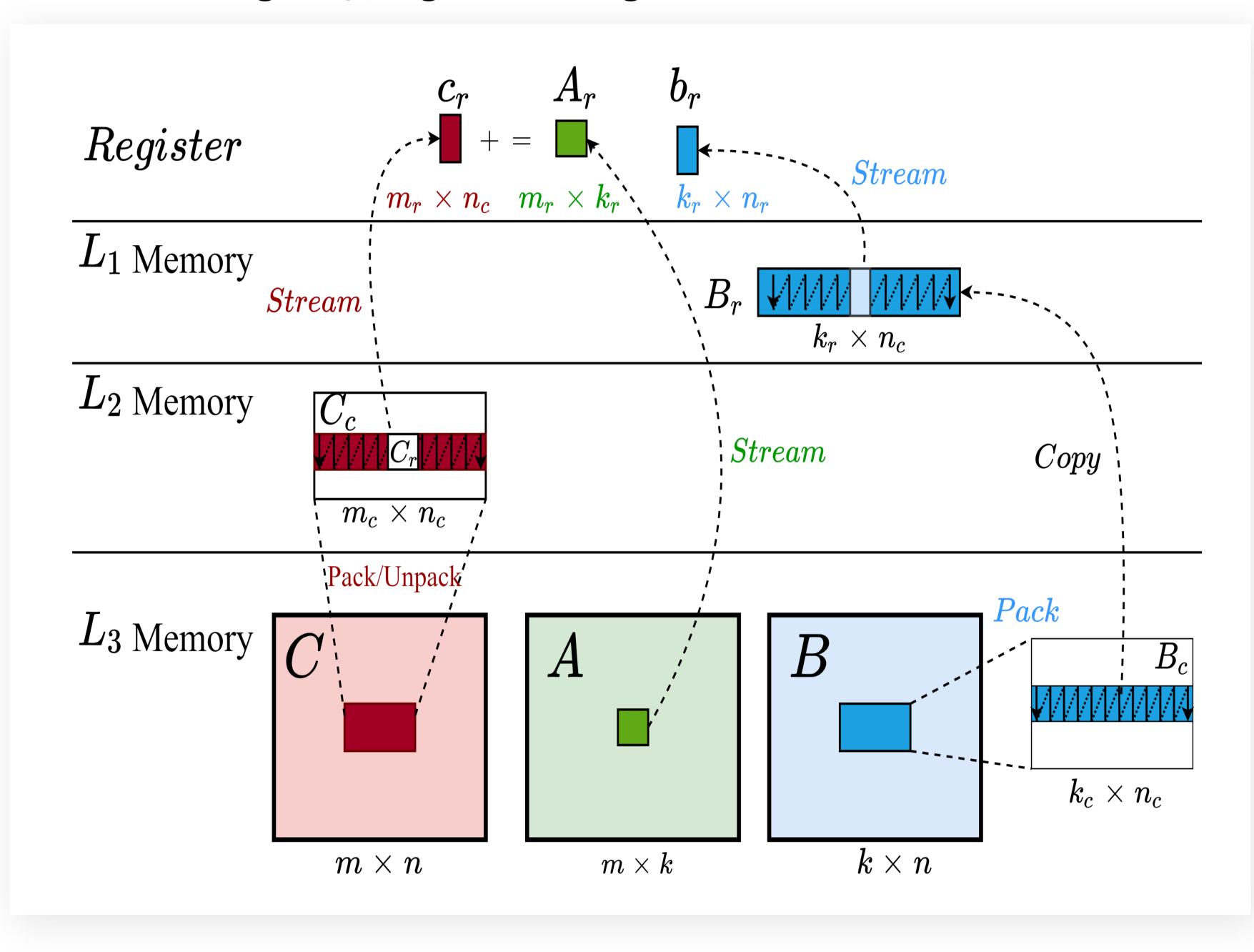
## GAP8 **Memory** Architecture



### **Proposed** GEMM algorithm (B3C2A0)

L1	for $(j_c = 0; j_c < n; j_c += n_c)$
L2	for $(p_c = 0; p_c < k; p_c += k_c)$ {
	$B_c \leftarrow B(p_c: p_c + k_c - 1, j_c: j_c + n_c - 1); // \text{Pack}$
L3	for $(i_c = 0; i_c < m; i_c + m_c)$
	$C_c \leftarrow C(i_c : i_c + m_c - 1, j_c : j_c + n_c - 1); // Pack$
L4	for $(p_r = 0; p_r < k_c; p_r + k_r)$
L5	for $(i_r = 0; i_r < m_c; i_r += m_r)$
L6	for $(j_r = 0; j_r < n_c; j_r += 1) //$ Micro-kernel
	$C_{c}(i_{r}:i_{r}+m_{r}-1,j_{r})$
	$+= A_c(i_r:i_r+m_r-1,p_r:p_r+k_r-1)$
	$\cdot B_c(p_r:p_r+k_r-1,j_r);$
	$C(i_c: i_c + m_c - 1, j_c: j_c + n_c - 1) \leftarrow C_c; // \text{Unpack}$
	}}
Proposed micro-Kernel (Loop 6)	
ger	<pre>mm_ukernel_ABresident_gap8( int nc, signed char *A, int ldA, signed char Br , signed char Cc</pre>
) (	
	nt jr, baseCB = 0;
v4	
	Is A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar
1	Is AO, A1, A2, A3, // Columns of the 4x4 micro-tile Ar br, cr; // Columns of Br, Cr
	Is A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar
reg	<pre>As A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar br, cr; // Columns of Br, Cr / Load the columns of the 4x4 micro-tile Ar into vector</pre>
rec // A(	<pre>As A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar br, cr; // Columns of Br, Cr / Load the columns of the 4x4 micro-tile Ar into vector gisters / Simulated in software using the v4s datatype ) = ((v4s) (&amp;A[0]); A1 = ((v4s) (&amp;A[Alda]);</pre>
rec // A(	<pre>As A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar br, cr; // Columns of Br, Cr / Load the columns of the 4x4 micro-tile Ar into vector gisters / Simulated in software using the v4s datatype</pre>
rec // A( A2	<pre>As A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar br, cr; // Columns of Br, Cr / Load the columns of the 4x4 micro-tile Ar into vector gisters / Simulated in software using the v4s datatype D = ((v4s ) (&amp;A[0]); A1 = ((v4s ) (&amp;A[Alda] );</pre>
rec // A( A2	<pre>As A0, A1, A2, A3, // Columns of the 4x4 micro-tile Ar br, cr; // Columns of Br, Cr / Load the columns of the 4x4 micro-tile Ar into vector gisters / Simulated in software using the v4s datatype 0 = ((v4s) (&amp;A[0]); A1 = ((v4s) (&amp;A[Alda]); 2 = ((v4s) (&amp;A[2*Alda]); A3 = ((v4s) (&amp;A[3*Alda]);</pre>

# Matrix Packing, Copying, Streaming



// Load the jr-th columns of Cr, Br into two vector registers

cr = ((v4s) (&Cr[baseCB]);

#### br = ((v4s) (&Br[baseCB]);

// Update i-th entry of cr as cr[i] += Ai \* br, i=0,1,2,3, // The GAP8 dot product is realized in software via the // gap8 dotp4 instruction cr[0] += gap8\_dotp4(A0, br); cr[1] += gap8\_dotp4(A1, br);

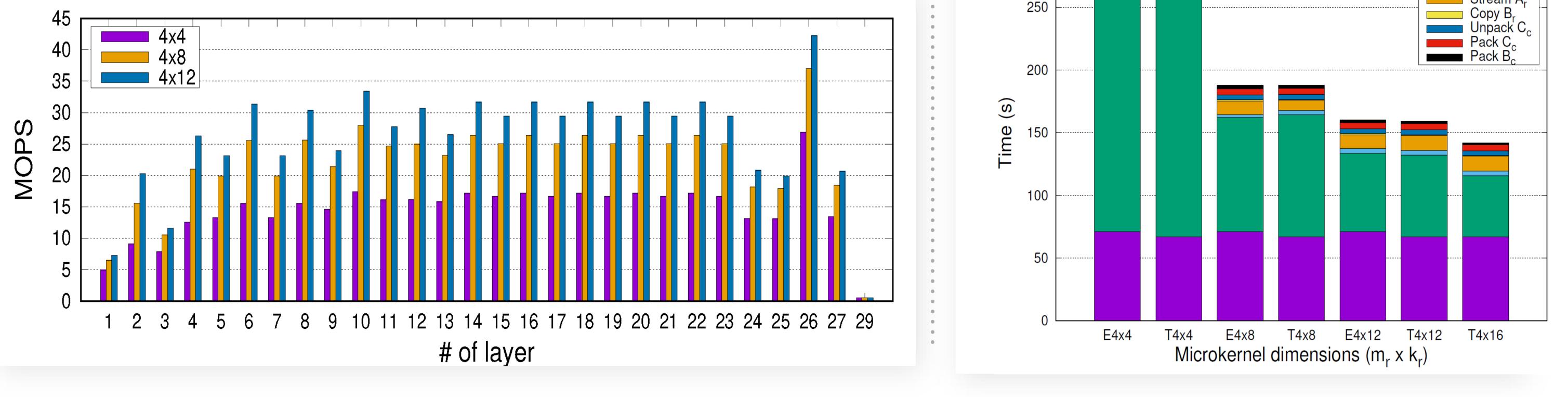
cr[2] += gap8\_dotp4(A2, br); cr[3] += gap8\_dotp4(A3, br);

// Store the column of Cr in memory. No vector support in GAP8

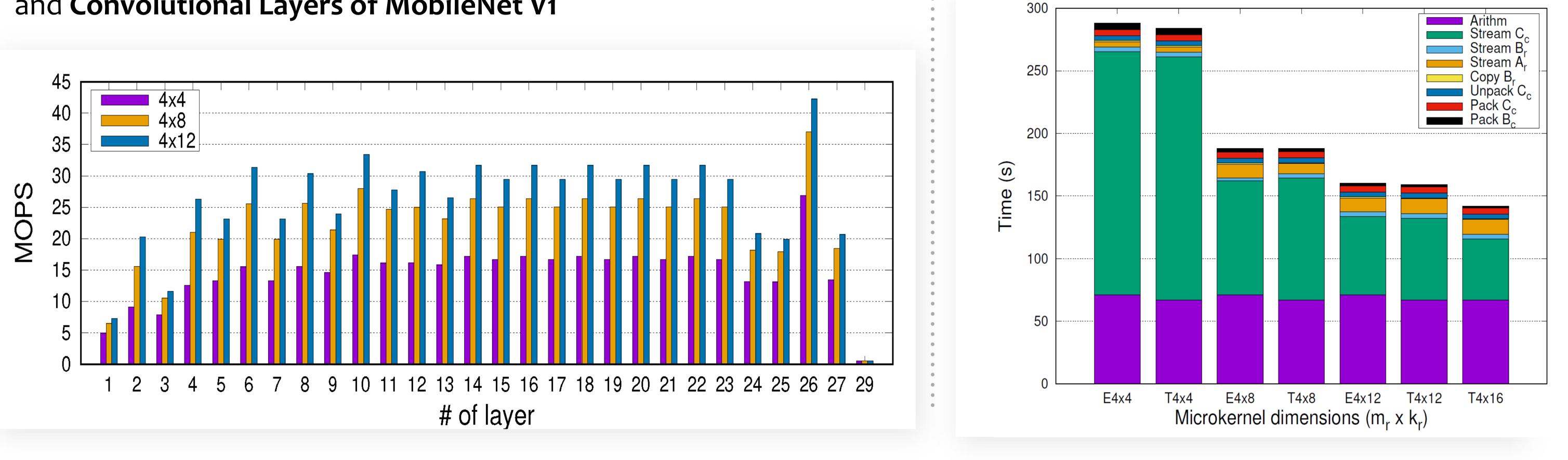
Cr[baseCB+0] = cr[0]; Cr[baseCB+1] = cr[1];Cr[baseCB+2] = cr[2]; Cr[baseCB+3] = cr[3];

baseCB += 4; // Prepare for next iteration

Performance on Different **Dimension of Microkernel** and Convolutional Layers of MobileNet V1



#### Runtimes on Different micro-kernel dimensions



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